Amendments to the Drawings

The attached sheets of drawings includes changes to Figs. 14 and 15. In Figs. 14 and 15, the legend "Prior Art" is added.

REMARKS

Initially, in the Office Action dated August 9, 2005, the Examiner has objected to Figs. 14 and 15. Claims 1 and 3 have been rejected under 35 U.S.C. §112, second paragraph. Claims 1 and 5 have been rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,845,409 (Talagala et al.). Claim 2 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Talagala et al. in view of U.S. Patent No. 6,532,547 (Wilcox). Claim 4 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Talagala et al. in view of Applicant's Admitted Prior Art (AAPA). Claim 6 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Talagala et al. in view of AAPA and further in view of U.S. Patent Publication No. 2003/0053772 A1 (Ikunishi et al.).

By the present response, Applicants have amended Figs. 14 and 15. Further, Applicants have canceled claims 7 and 8 without disclaimer. Moreover, Applicants have amended claims 1-4 to further clarify the invention. Claims 1-6 remain pending in the present application.

Drawings Objections

Figs. 14 and 15 have been objected to as the Examiner requires that they be designated by a legend such as "Prior Art". Applicants have complied with this request and submitted amended figures. Accordingly, Applicants respectfully request that these objections be withdrawn.

35 U.S.C. §112 Rejections

Claims 1 and 3 have been rejected under 35 U.S.C. §112, second paragraph. Applicants have amended the claims of the present application to further clarify the invention and respectfully request that these rejections be withdrawn.

35 U.S.C. §102 Rejections

Claims 1 and 5 have been rejected under 35 U.S.C. §102(e) as being anticipated by Talagala et al. Applicants respectfully traverse these rejections.

Talagala et al. discloses a switch including a host input/output (I/O) port adapted for coupling to a controller, multiple device I/O ports each adapted for coupling to at least one device, and logic coupled between the host I/O port and the device I/O ports configured to selectively form a communication channel between the host I/O port and one of the device I/O ports. The switch may operate in a connected mode and a disconnected mode. When the switch is in the disconnected mode, the logic may not form a communication channel between the host I/O port and any of the device I/O ports.

Regarding claim 1, Applicants submit that Talagala et al. does not disclose or suggest the limitations in the combination of, inter alia, a disk array device that includes: a channel adapter that controls data transmission with a high-order device located external to the disk array device, a storage device control board to which the storage device is connected, a disk adapter that is connected to the storage device via the storage device control board and controls data transmission and reception with the storage device, or a management unit that is respectively connected to the

disk adapter and the channel adapter wherein switch circuits that are respectively disposed at an input side and an output side of the connection circuit are switchable between a connected mode where they are connected to an adjacent storage device control board and an independent mode where they are separated from the adjacent storage device control board, or where the switch circuits are switchable between the connected mode and the independent mode by an output signal from the management unit. Applicants assert that the Examiner has misinterpreted the Talagala et al. reference. For example, the Examiner asserts that Talagala et al. teaches a disk array unit by Talagala et al.'s Fig. 2, however, this figure merely discloses a diagram of a computer system where the processing unit is coupled to two switches in a series cascaded arrangement. Fig. 2 in Talagala et al. discloses a computer system. This is not a disk array device, as recited in the claims of the present application. Everything disclosed in Talagala et al. supports that Talagala et al. is clearly only related to a processing unit, including the title of the invention, the abstract, the description, and the claims, and has nothing to do with a disk array device.

Moreover, the Examiner asserts that Talagala et al. discloses a channel adapter by Talagala et al.'s disclosure in Fig. 2 of element 14A. However, element 14A is merely a switch that is connected to a second switch 14B in a series cascaded arrangement (see, col. 8, lines 3-7). This is not a channel adapter that is included in a disk array device, as recited in the claims of the present application.

Further, the Examiner asserts that Talagala et al. discloses a channel adapter controlling data transmission and reception with a high order device by its disclosure of element 32 in Fig. 2. However, element 32 is merely a CPU that is part of a processor unit. Further, the CPU and processing unit are all a part of the computer system 10 of Fig. 2 (that the Examiner has asserted is a disk array device). This is not a high order device located external to the disk array device, as recited in the claims of the present application. Element 32 is a CPU part of a processing unit that is a part of the computer system 10, and is not external to the computer system 10.

In addition, the Examiner asserts that Talagala et al. discloses a storage device control board to which the storage device is connected at Fig. 2, element 14A, Fig. 3, element 40, and col. 8, lines 52-61. However, Fig. 3A, element 40 are merely details of switch 14A, which the Examiner has already previously asserted is Applicants' claimed channel adapter. This implies that Applicants' claimed storage device control board is a part of the channel adapter. This is incorrect in that the channel adapter and the storage device control board are both a part of the disk array device. The Examiner appears to assert that element 14A in Fig. 2 is both Applicants' claimed channel adapter and storage device control board or that element 40 in element 14A is Applicants' claimed storage device control board. Either interpretation is a total mischaracterization of the Talagala et al. reference as it applies to the limitations in the claims of the present application.

Moreover, the Examiner asserts that Talagala et al. discloses a disk adapter that is connected to the storage device via the storage device control board in

Talagala et al. in Fig. 2, element 16 and Fig. 2, element 30, as well as Fig. 2, element 14A including element 40 in Fig. 3. However, element 16 in Fig. 2 of Talagala et al. is merely a controller that is a part of the processor unit 12. This is not a disk adapter that is part of a disk array device, as recited in the claims of the present application. Moreover, as noted previously, element 14A in Fig. 2 of Talagala et al. is not a storage device control board.

The Examiner asserts that Talagala et al. discloses a management unit in Figs. 1 and 2, element 12, which is respectively connected to the disk adapter, Figs. 1 and 2, element 16, and the channel adapter, Figs. 1 and 2, element 14A. However, as has been previously noted, element 16 in Fig. 2 is not a disk adapter, as recited in the claims of the present application, and element 14A in Fig. 2 is not a channel adapter, as recited in the claims of the present application.

Since, as noted previously, element 14A of Fig. 2 of Talagala et al. is not a channel adapter and element 40 in Fig. 3A is not a storage device control board, Talagala et al. does not disclose or suggest a storage device control board that includes a connection circuit, switch circuits disposed at an input side and an output side of the connection circuit, or switch circuits being switchable between the connected mode and the independent mode via an output signal from the management unit, as recited in the claims of the present application. The Examiner asserts that Talagala et al. discloses switch circuits that are respectively disposed at an input side and an output side of the connection circuit by element 47 of Fig. 3B. However, element 47 in Talagala et al. merely discloses switching elements that are

coupled between host I/O port 18 and device I/O ports 20A-20C (see col. 9, lines 10-11). This is not switching circuits respectively disposed at an input side and an output side of a connection circuit, as recited in the claims of the present application. The Examiner further asserts that Talagala et al. discloses switch circuits between a connected mode where they are connected to another adjacent storage device control board and an independent mode where they are separated from the other adjacent storage device control board with element 14B and at col. 9, lines 25-36. However, this portion of Talagala et al. merely discloses that switch 14 operates in a connected mode and a disconnected mode, where in the disconnected mode logic 40 does not form a communication channel between host I/O port 18 and any device I/O port 20, and when in connected mode the switch 14 provides a communication channel between host I/O port 18 and the selected one of the device I/O ports 20. This is not switch circuits respectively disposed at an input side and an output side of the connection circuit being switchable between a connected mode where they are connected to another adjacent storage device control board, and an independent mode where they are separated from the adjacent storage device control board, as recited in the claims of the present application. Talagala et al. merely discloses switch 14 acting as a typical switch and providing or not providing a connection between processing unit 12 and device 30. Talagala et al. does not disclose or suggest anything related to a switch circuit being in a connected mode connecting to an adjacent storage device control board. Further, Talagala et al. does not disclose or suggest the switch circuits being switchable between the connected mode and the

independent mode by an output signal from a management unit that is part of a disk array device, as recited in the claims of the present application.

Regarding claim 5, Applicants submit that this claim is dependent on independent claim 1 and, therefore, is patentable at least for the same reasons noted previously regarding this independent claim. For example, Applicants submit that Talagala et al. does not disclose or suggest where the connection circuit is configured by any of a port bypass circuit and a fibre channel switch.

Accordingly, Applicants submit that Talagala et al. does not disclose or suggest the limitations in the combination of each of claims 1 and 5 of the present application. Applicants respectfully request that these rejections be withdrawn and that these claims be allowed.

35 U.S.C. §103 Rejections

Claim 2 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Talagala et al. in view of Wilcox. Applicants respectfully traverse this rejection.

Wilcox discloses a redundant peripheral device subsystem in a computer system including first and second peripheral device controllers. First and second peripheral busses are coupled to the first and second peripheral device controllers, respectively. A controllable switch is coupled between the first and second peripheral device busses. The controllable switch either isolates the first and second peripheral device busses from each other, or joins them into a single peripheral device bus.

Applicants submit that claim 2 is dependent on independent claim 1 and, therefore, is patentable at least for the same reasons noted previously regarding this independent claim. Applicants submit that Wilcox does not overcome the substantial defects noted previously regarding Talagala et al. For example, Applicants submit that none of the cited references disclose or suggest where the storage device control board and the adjacent storage device control board are mounted on a same attachment-use board.

Accordingly, Applicants submit that none of the cited references, taken alone or in any proper combination, disclose, suggest or render obvious the limitations in the combination of claim 2 of the present application. Applicants respectfully request that this rejection be withdrawn and that this claim be allowed.

Claim 4 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Talagala et al. in view of AAPA. Applicants respectfully traverse this rejection.

AAPA as cited by the Examiner from Applicants' Background of the Invention merely refers to Fig. 15, elements 601, 602, and 610-612, A port, and B port.

Applicants submit that claim 4 is dependent on independent claim 1 and, therefore, is patentable at least for the same reasons noted previously regarding this independent claim. Applicants submit that the cited AAPA does not overcome the substantial defects noted previously regarding Talagala et al. For example, Applicants submit that none of the cited references disclose or suggest where the storage device includes a first port and a second port, with the first port and the second port being connected to respectively different storage device control boards

and the different storage device control boards being connected to respectively different disk adapters.

Accordingly, Applicants submit that none of the cited references, taken alone or in any proper combination, disclose, suggest or render obvious the limitations in the combination of claim 4 of the present application. Applicants respectfully request that this rejection be withdrawn and that this claim be allowed.

Claim 6 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Talagala et al. in view of AAPA and further in view of Ikunishi et al. Applicants respectfully traverse this rejection.

Ikunishi et al. discloses an optical fiber sheet being provided with a plurality of input ports, each constituted by an optical fiber group, a plurality of output ports, each constituted by an optical fiber group made of optical fibers selected from a plurality of optical fibers extending from the plurality of input ports, and a sheet substrate on which the plurality of optical fibers extending from the plurality of output ports is arranged. The plurality of optical fibers includes an optical fiber provided with an identification means that allows identification of the input port side portion and the output port side portion by visual confirmation.

Applicants submit that claim 6 is dependent on independent claim 1 and, therefore, is patentable at least for the same reasons noted previously regarding this independent claim. Applicants submit that neither the AAPA or Ikunishi et al. overcome the substantial defects noted previously regarding Talagala et al. For example, Applicants submit that none of the cited references disclose or suggest

where respectively different colors are associated with input-side connectors and output-side connectors with which the disk adapter and the storage device control board are disposed, or respectively different colors being associated with signal lines associated with the first port and signal lines associated with the second port of signal lines connecting the respective connectors to each other.

Accordingly, Applicants submit that none of the cited references, taken alone or in any proper combination, disclose, suggest or render obvious the limitations in the combination of claim 6 of the present application. Applicants respectfully request that this rejection be withdrawn and that this claim be allowed.

In view of the foregoing amendments and remarks, Applicants submit that claims 1-6 are now in condition for allowance. Accordingly, early allowance of such claims is respectfully requested.

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of Mattingly, Stanger, Malur & Brundidge, P.C., Deposit Account No. 50-1417 (referencing attorney docket no. 1309.43598X00).

Respectfully submitted,

MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C.

Carl I. Brundidge
Registration No. 29,621

CIB/sdb
(703) 684-1120

Attachment: Replacement Sheet